In the Claims

Applicants have submitted a new claim set showing amended claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please add new claims 10-45 as shown below.

1. (Previously presented) A phase-locked loop including:

an oscillator, controlled by a control signal generated by a comparison circuit comparing a reference frequency with an oscillator frequency and filtered by an integrator low-pass filter;

a control and adjustment circuit for, with a predetermined frequency smaller than the reference frequency, taking into account the value of the filtered controlled signal and, if this value is out of a range of predetermined values, adjusting the operating range of the oscillator; and

an inhibition circuit for deactivating the comparison circuit for a predetermined duration before taking into account the value of the filtered control signal.

2. (Previously presented) The phase-locked loop of claim 1, wherein the inhibition circuit is activated only if the value of the filtered control signal is out of the range of predetermined values.

3. (Previously presented) The phase-locked loop of claim 1, wherein the oscillator, the comparison circuit, the control and adjustment circuit, and the inhibition circuit are made in an integrated circuit.

4. (Previously presented) The phase-locked loop of claim 1, wherein the filter includes a first capacitor connected in series with a first resistor between an input/output terminal and a ground, a second capacitor, of small capacitance as compared to the first capacitor, being connected between the input/output terminal and the ground.

5. (Previously presented) The phase-locked loop of claim 1, wherein the comparison circuit includes first and second D flip-flops respectively rated at the reference frequency and at

a variable frequency equal to a predetermined ratio of the oscillator frequency, the input terminals of the D flip-flops being connected to 1, the output terminal of the first flip-flop generating an incrementation signal, the output terminal of the second flip-flop generating a decrementation signal, a reset terminal of the D flip-flops being activable by a NAND combination of the incrementation and decrementation signals, the output terminal of the comparison circuit being connected via a first switch to a source of a positive constant current, the first switch being respectively on or off when the incrementation signal is at 1 or 0, the output terminal of the comparison circuit being further connected via a second switch to a source of a negative constant current, the second switch being respectively on or off when the decrementation signal is at 1 or at 0.

6. (Previously presented) The phase-locked loop of claim 5, wherein the oscillator includes an amplifier with a negative resistance, the output of which is the oscillator output, the input of the amplifier being connected to a first terminal of a third capacitor, the second terminal of the third capacitor being connected to the oscillator input via a second resistor, a varicap diode being connected by its cathode to the second terminal of the third capacitor, the anode of the varicap diode being connected to ground, an inductance and a variable capacitor being connected in parallel between the input of the amplifier and the ground, the capacitance of the variable capacitor being controlled by an adjustment signal.

7. (Previously presented) The phase-locked loop of claim 6, wherein the control and adjustment circuit includes a first comparator enabling comparison of the filtered control signal with a high predetermined voltage, a second comparator enabling comparison of the filtered control signal with a low predetermined voltage, the first and second comparators controlling a coding block which controls via an adder the incrementation or the decrementation of the adjustment signal, stored in a third D flip-flop clocked at said predetermined frequency by a clock signal.

8. (Previously presented) The phase-locked loop of claim 7, wherein the inhibition circuit includes a fourth D flip-flop generating an inhibition signal, the fourth flip-flop being

clocked by the inverse of the clock signal and reset by the high state of the clock signal, the input terminal of the fourth D flip-flop receiving a signal equal to 1 when the control signal is greater than the high predetermined voltage or smaller than the low predetermined voltage, and equal to 0 otherwise, and two AND gates arranged to cancel the incrementation and decrementation signals respectively provided by the first and second D flip-flops to the first and second switches when the inhibition signal is equal to 1.

9. (Previously presented) A method for controlling a phase-locked loop including an oscillator controlled by a control signal generated by a comparison circuit comparing a reference frequency with the oscillator frequency and filtered by an integrator low-pass filter, including the steps of:

taking into account the value of the filtered control signal with a predetermined frequency smaller than the reference frequency and adjusting the operating range of the oscillator if the value of the filtered control signal is out of a range of predetermined values; and

deactivating the comparison circuit during a predetermined duration before taking into account the value of the filtered control signal.

10. (New) A phase-locked loop configured to provide an output signal, the phase-locked loop comprising:

a comparison circuit configured to compare a reference signal and the output signal;

an inhibition circuit connected to the comparison circuit, wherein the inhibition circuit comprises a D flip-flop configured to output an inhibit signal to the comparison circuit; and

a frequency divider coupled to the inhibition circuit.

11. (New) The phase-locked loop of claim 10, wherein the phase-locked loop is at least part of an integrated circuit.

12. (New) The phase-locked loop of claim 10, further comprising a low-pass filter configured to filter an output of the comparison circuit.

13. (New) The phase-locked loop of claim 10, wherein the phase-locked loop is capable of operating in a plurality of frequency ranges.

14. (New) The phase-locked loop of claim 13, wherein at least two of the plurality of frequency ranges are overlapping.

15. (New) The phase-locked loop of claim 10, further comprising:

a voltage controlled oscillator configured to produce the output signal.

16. (New) The phase-locked loop of claim 15, wherein the phase locked loop is capable of operating in a plurality of frequency ranges, the phase-locked loop further comprising:

a control and adjustment circuit configured to sample an input to the voltage controlled oscillator and adjust an operating frequency range of the phase-locked loop.

17. (New) The phase-locked loop of claim 10, wherein a clock input of the D flip-flop is configured to receive an inverted output from the frequency divider.

18. (New) The phase-locked loop of claim 10, wherein a reset input of the D flip-flop is configured to receive an output of the frequency divider.

19. (New) The phase-locked loop of claim 10, wherein a D input of the D flip-flop is connected to a voltage supply.

20. (New) The phase-locked loop of claim 10, wherein the inhibition circuit is configured to receive a high reference voltage and a low reference voltage.

21. (New) The phase-locked loop of claim 20, wherein the inhibition circuit comprises first comparator having an inverting input configured to receive the high reference voltage.

22. (New) The phase-locked loop of claim 21, wherein the inhibition circuit further comprises a second comparator having a non-inverting input configured to receive the low reference voltage.

23. (New) The phase-locked loop of claim 22, wherein a D input of the D flip-flop is configured to receive a logical combination of an output of the first comparator and an output of the second comparator.

24. (New) The phase-locked loop of claim 23, wherein the logical combination is an OR combination.

25. (New) The phase-locked loop of claim 23, further comprising:

a voltage controlled oscillator configured to receive a control signal;

wherein a non-inverting input of the first comparator and an inverting input of the second comparator are configured to receive the control signal.

26. (New) The phase-locked loop of claim 25, wherein the phase-locked loop is at least part of an integrated circuit.

27. (New) A method of operating a phase-locked loop comprising a voltage controlled oscillator controlled by a control signal, the method comprising:

monitoring a value of the control signal; and

inhibiting the phase-locked loop if the monitored value of the control signal is outside a predetermined range of values.

28. (New) The method of claim 27, wherein the phase-locked loop is inhibited if the monitored value of the control signal is greater than a first reference value.

29. (New) The method of claim 28, wherein the phase-locked loop is inhibited if the monitored value of the control signal is less than a second reference value.

30. (New) The method of claim 29, wherein the first reference value is greater than the second reference value.

31. (New) The method of claim 27, wherein the phase-locked loop further comprises a comparison circuit to compare an output of the voltage controlled oscillator and a reference signal, and wherein inhibiting the phase-locked loop comprises inhibiting the comparison circuit.

32. (New) The method of claim 27, further comprising:

sampling a value of the control signal in addition to monitoring the control signal.

33. (New) The method of claim 32, further comprising:

operating the phase locked loop in a first frequency range; and

if the sampled value of the control signal is outside a second predetermined range of values, operating the phase-locked loop in a second frequency range.

34. (New) The method of claim 33, wherein the predetermined range of values and the second predetermined range of values are the same.

35. (New) The method of claim 27, wherein inhibiting the phase-locked loop comprises opening the phase-locked loop.

36. (New) The method of claim 35, wherein the phase-locked loop further comprises a comparison circuit to compare an output of the voltage controlled oscillator and a reference signal, and wherein opening the phase-locked loop comprises inhibiting the comparison circuit.

37. (New) A method of operating a phase-locked loop comprising a voltage controlled oscillator controlled by a control signal, the method comprising:

sampling a value of the control signal; and

inhibiting the phase-locked loop prior to sampling the value of the control signal.

38. (New) The method of claim 37, wherein the inhibition of the phase-locked loop lasts for a predetermined amount of time.

39. (New) The method of claim 37, wherein the control signal is sampled periodically.

40. (New) The method of claim 39, wherein the inhibition of the phase-locked loop is performed periodically.

41. (New) The method of claim 40, wherein the inhibition of the phase-locked loop and the sampling of the control signal occur at a same frequency.

42. (New) The method of claim 37, wherein the phase-locked loop further comprises a comparison circuit to compare an output of the voltage controlled oscillator and a reference signal, and wherein inhibiting the phase-locked loop comprises inhibiting the comparison circuit.

43. (New) The method of claim 37, further comprising:

operating the phase locked loop in a first frequency range; and

if the sampled value of the control signal is outside a predetermined range of values, operating the phase-locked loop in a second frequency range.

44. (New) The method of claim 37, wherein inhibiting the phase-locked loop comprises opening the phase-locked loop.

45. (New) The method of claim 44, wherein the phase-locked loop further comprises a comparison circuit to compare an output of the voltage controlled oscillator and a reference signal, and wherein opening the phase-locked loop comprises inhibiting the comparison circuit.